DATASHEET

Radiation Hardened 30V 32-Channel Analog Multiplexer

ISL71841SEH

The ISL71841SEH is a radiation hardened, 32-channel high ESD protected multiplexer that is fabricated using Intersil's proprietary P6SOI (Silicon On Insulator) process technology to mitigate single event effects. It operates with a dual supply voltage ranging from ±10.8V to ±16.5V. It has a 5-bit address plus an enable pin that can be driven with adjustable logic thresholds to conveniently select 1 of 32 available channels. An inactive channel is separated from an active channel by a high impedance, which inhibits any interaction between them.

The ISL71841SEH's low r_{ON} allows for improved signal integrity and reduced power losses. The ISL71841SEH is also designed for cold sparing making it excellent for high reliability applications that have redundancy requirements. It is designed to provide a high impedance to the analog source in a powered off condition, making it easy to add additional backup devices without loading signal sources. The ISL71841SEH also incorporates input analog overvoltage protection, which will disable the switch to protect downstream devices.

The ISL71841SEH is available in a 48 Ld CQFP or die form and operates across the extended temperature range of -55°C to +125°C.

There is also a 16-channel version available offered in a 28 Ld CDFP, please refer to the ISL71840SEH datasheet for more information. For a list of differences please refer to Table 1 on page 3.

Related Literature

- UG037, "ISL71841SEHEV1Z Evaluation Board User Guide"
- TR007, "Single Event Effects (SEE) Testing of the ISL71841SEH 32:1 30V Multiplexer"
- TR011, "Total Dose Testing of the ISL71841SEH 32-channel Analog Multiplexer"

Features

- DLA SMD# 5962-15220
- Fabricated using P6SOI process technology
  - Provides latch-up immunity
- ESD protection 8kV (HBM)
- Rail-to-rail operation
- Overvoltage protection
- Low r_{ON} . . . . <500Ω (typical)
- Flexible split rail operation
  - Positive supply above GND (V^+) . . . . +10.8V to +16.5V
  - Negative supply below GND (V^-) . . . . -10.8V to -16.5V
- Adjustable logic threshold control with VREF pin
- Cold sparing capable (from ground). . . . . ±25V
- Analog overvoltage range (from ground). . . . . ±35V
- Off switch leakage . . . . 100nA (maximum)
- Transition times (t_R, t_F) . . . . 500ns (typical)
- Break-before-make switching
- Grounded metal lid (internally connected)
- Operating temperature range. . . . . -55°C to +125°C
- Radiation tolerance
  - High dose rate (50-300rad(Si)/s). . . . . 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . 100krad(Si) (Note)
  - SEB LET_{TH} . . . . 86.4MeV•cm²/mg

NOTE: Product capability established by initial characterization. All subsequent lots are assurance tested to 50krad (0.01rad(Si)/s) wafer-by-wafer.

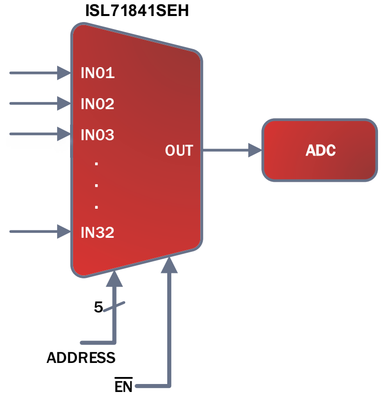


FIGURE 1. TYPICAL APPLICATION

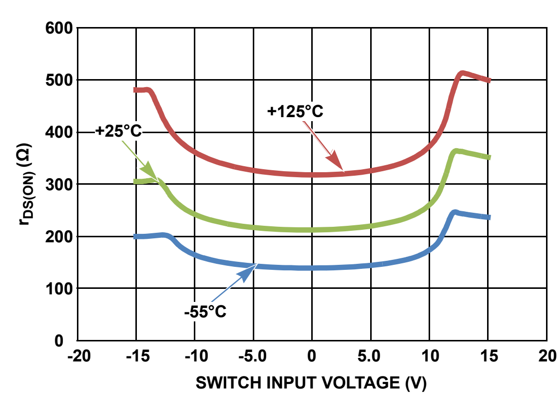


FIGURE 2. $r_{DS(ON)}$ vs POWER SUPPLY ACROSS SWITCH INPUT COMMON MODE VOLTAGE AT +25°C

Table of Contents

Ordering Information

ORDERING NUMBER (Note 2)	PART NUMBER (Note 1)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962R1522001VXC	ISL71841SEHVF	-55 to +125	48 LD CQFP	R48.A
ISL71841SEHF/PROTO	ISL71841SEHF/PROTO	-55 to +125	48 LD CQFP	R48.A
5962R1522001V9A	ISL71841SEHVX	-55 to +125	DIE	
ISL71841SEHX/SAMPLE	ISL71841SEHX/SAMPLE	-55 to +125	DIE	
ISL71841SEHEV1Z	Evaluation Board			

NOTES:

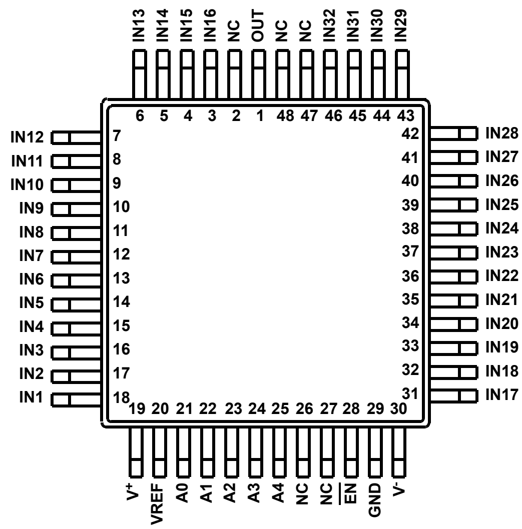
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table must be used when ordering.

TABLE 1. TABLE OF DIFFERENCES

SPEC	ISL71840SEH	ISL71841SEH
Number of Channels	16	32
Supply Current (I+/I-)	350µA (Max)	400µA (Max)
Output Leakage (+125°C)	60nA (Max)	120nA (Max)

Pin Configuration

ISL71841SEH
(48 LD CQFP)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
NC	2, 26, 27, 47, 48	Not connected, no internal connection.
OUT	1	Output for multiplexer
V^+	19	Positive power supply
V^-	30	Negative power supply
INx	3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46	Inputs for multiplexer
Ax	21, 22, 23, 24, 25	Address lines for multiplexer
$\overline{EN}$	28	Enable control for multiplexer (active low)
VREF	20	Reference voltage used to set logic thresholds
GND	29	Ground
LID	NA	Package Lid is internally connected to GND (Pin 29)

Absolute Maximum Ratings

Positive Supply Voltage above GND (V^+) (Note 5) . . . . +20V
Negative Supply Voltage below GND (V^-) (Note 5) . . . . -20V
Maximum Supply Voltage Differential (V^+ to V^-) (Note 5) 40V
Analog Input Voltage (INx)
From GND (Note 5) . . . . ±35V
Digital Input Voltage Range ($\overline{EN}$, Ax) . . . . GND to V^+
VREF to GND (Note 5) 16.5V
ESD Tolerance
Human Body Model (Tested per MIL-STD-883 TM 3015) 8kV
Charged Device Model (Tested per JESD22-C101D) 250V
Machine Model (Tested per JESD22-A115-A). 250V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld CQFP (Notes 3, 4)	50	2

Storage Temperature Range. . . . .-65°C to +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . .-55°C to +125°C
Maximum Operating Junction Temperature . . . .+150°C
Positive Supply Voltage Above GND (V^+) . . . . +10.8V to +16.5V
Negative Supply Voltage Below GND (V^-). . . . .-10.8V to -16.5V
Supply Voltage Differential (V^+ to V^-) . . . . 21.6V to 33V
VREF to GND . . . . 4.5V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the package underside.
5. Tested in a heavy ion environment at LET = 86.3MeV • cm²/mg at +125°C.

Electrical Specifications (±15V)

V^+ = 15V, V^- = -15V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_S	Analog Input Signal Range		V^-	-	V^+	V
r_{ON}	Channel ON-Resistance	V± = ±15.0V, ±16.5V I_{OUT} = -1mA, V_{IN} = +5V, -5V	-	-	**500**	Ω
		V± = ±15.0V, ±16.5V I_{OUT} = -1mA, V_{IN} = V^+, V^-	-	-	**700**	Ω
Δr_{ON}	r_{ON} Match Between Channels	V_{IN} = +5V, -5V; I_{OUT} = -1mA	-	10	**20**	Ω
$R_{FLAT(ON)}$	ON-Resistance Flatness	V_{IN} = +5V, -5V	-	-	**25**	Ω
$I_{S(OFF)}$	Switch Off Leakage	V_{IN} = V^+ - 5V, V± = ±16.5V All unused inputs are tied to V^- + 5V	**-10**	-	**10**	nA
		Post radiation	-100	-	100	nA
		V_{IN} = V^- + 5V, V± = ±16.5V All other inputs = V^+ - 5V T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-100	-	100	nA
$I_{S(OFF)\ POWER\ OFF}$	Switch Off Leakage with Device Powered Off	V_{IN} = +25V, V± = $V_{\overline{EN}}$ = V_A = V_{REF} = 0V T_A = +25°C, V± = 0V	-10	-	10	nA
		T_A = -55°C, +125°C	-10	-	80	nA
		Post radiation	-100	-	100	nA
		V_{IN} = -25V, V± = $V_{\overline{EN}}$ = V_A = V_{REF} = 0V T_A = +25°C, V± = 0V	-10	-	10	nA
		T_A = -55°C, +125°C	-80	-	10	nA
		Post radiation	-100	-	100	nA

Electrical Specifications (±15V) V^+ = 15V, V^- = -15V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.** (Continued)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$I_{S(OFF)\ POWER\ OFF}$	Switch Off Leakage with Device Powered Off	V_{IN} = +25V, $V_{\overline{EN}}/V_A/V_{REF}$ = 0V V± = OPEN, T_A = +25°C	-10	-	10	nA
		T_A = -55°C, +125°C	-10	-	80	nA
		Post radiation	-100	-	100	nA
		V_{IN} = -25V, $V_{\overline{EN}}/V_A/V_{REF}$ = 0V V± = OPEN, T_A = +25°C	-10	-	10	nA
		T_A = -55°C, +125°C	-80	-	10	nA
		Post radiation	-100	-	100	nA
$I_{S(ON)\ OVERVOLT}$	Switch On Leakage Current Into the Source (overvoltage)	V_{IN} = +35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-80	-	80	nA
		Post radiation	-500	-	500	nA
		V_{IN} = -35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-500	-	500	nA
$I_{S(OFF)\ OVERVOLT}$	Switch Off Leakage Current Into the Source (overvoltage)	V_{IN} = +35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-80	-	80	nA
		Post radiation	-750	-	750	nA
		V_{IN} = -35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-750	-	750	nA
$I_{D(OFF)}$	Switch Off Leakage	V_{OUT} = V^+ - 5V, all inputs = V^- + 5V V± = ±16.5V, T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	0	-	120	nA
		Post radiation	-80	-	80	nA
		V_{OUT} = V^- + 5V, all inputs = V^+ - 5V V± = ±16.5V, T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	-120	-	0	nA
		Post radiation	-80	-	80	nA
$I_{D(OFF)\ OVERVOLT}$	Switch Off Leakage Current Into the Drain (overvoltage)	V_{OUT} = 0V, V_{IN} = +35V, V± = ±16.5V All unused inputs are tied to GND	**-10**	-	**10**	nA
		Post radiation	-500	-	500	nA
		V_{OUT} = 0V, V_{IN} = -35V, V± = ±16.5V All unused inputs are tied to GND	**-10**	-	**10**	nA
		Post radiation	-500	-	500	nA

Electrical Specifications (±15V)

V^+ = 15V, V^- = -15V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.** (Continued)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$I_{D(ON)}$	Switch On Leakage Current Into the Source/Drain	V_{IN} = V_{OUT} = V^+ - 5V, T_A = +25°C, -55°C All unused inputs = V^- + 5V, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	0	-	120	nA
		Post radiation	-100	-	100	nA
		V_{IN} = V_{OUT} = V^- + 5V, T_A = +25°C, -55°C All unused inputs = V^- + 5V, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-120	-	0	nA
		Post radiation	-100	-	100	nA
$V_{AH/L}$, $V_{ENH/L}$	Logic Input High/Low Voltage	V_{REF} = 5.0V	**1.2**	-	**1.6**	V
I_{AH}, I_{ENH}	Input Current with V_{AH}, V_{ENH}	V_A = $V_{\overline{EN}}$ = 4.0V V^+= 16.5V, V^- = -16.5V	**-100**	-	**100**	nA
I_{AL}, I_{ENL}	Input Current with V_{AL}, V_{ENL}	V_A = $V_{\overline{EN}}$ = 0.8V V+ = 16.5V, V^- = -16.5V	**-100**	-	**100**	nA
I+	Quiescent Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	-	-	**400**	µA
I-	Quiescent Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	**-400**	-		µA
I+	Standby Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	-	-	**400**	µA
I-	Standby Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	**-400**	-		µA
I_{REF}	Supply Current into V_{REF}	V_{REF} = 5.5V, V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	**10**	-	**35**	µA
DYNAMIC						
t_{ALH}	Transition Time	Figures 4, 5	-	0.5	**800**	ns
t_{AHL}	Transition Time	Figures 4, 5	-	0.5	**800**	ns
t_{BBM}	Break-Before-Make Delay	Figures 8, 9	**5**	50	**200**	ns
		Post radiation	**5**	-	**400**	ns
t_{ENABLE}	Enable Turn-On Time	Figures 6, 7	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns
$t_{DISABLE}$	Disable Turn-Off Time	Figures 6, 7	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns
V_{CTE}	Charge Injection	C_L = 100pF, V_{IN} = 0V, (Figure 6)	-	2	5	pC
V_{ISO}	Off Isolation	$V_{\overline{EN}}$ = 4V, R_L = 1kΩ, f = 200kHz, C_L = 7pF, V_{RMS} = 3V	75	-	-	dB
V_{CT}	Crosstalk	$V_{\overline{EN}}$ = 0.8V, R_L = 1kΩ, f = 200kHz, C_L = 7pF, V_{RMS} = 3V	47	-	-	dB
C_A	Digital Input Capacitance	f = 1MHz, V^+ = V^- = 0V	-	-	**7**	pF
$C_{IN(OFF)}$	Input Capacitance	f = 1MHz, V^+ = V^- = 0V	-	-	**5**	pF
$C_{OUT(OFF)}$	Output Capacitance	f = 1MHz, V^+ = V^- = 0V	-	-	**50**	pF

Electrical Specifications (±12V) V^+ = 12V, V^- = -12V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_S	Analog Input Signal Range		V^-		V^+	V
r_{ON}	Channel ON-Resistance	V± = ±10.8V, ±13.2V I_{OUT} = -1mA, V_{IN} = +5V, -5V	-	-	**500**	Ω
		V± = ±10.8V, ±13.2V I_{OUT} = -1mA, V_{IN} = V^+, V^-	-	-	**700**	Ω
Δr_{ON}	r_{ON} Match Between Channels	V_{IN} = +5V, -5V; I_{OUT} = -1mA	-	10	**20**	Ω
$R_{FLAT(ON)}$	ON-Resistance Flatness	V_{IN} = +5V, -5V, V± = ±13.2V	-	-	**25**	Ω
		V_{IN} = +5V, -5V, V± = ±10.8V, T_A = +25°C, -55°C, +125°C	-	-	30	Ω
		V_{IN} = +5V, -5V, V± = ±10.8V, post radiation			**40**	Ω
I+	Quiescent Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	-	-	**400**	µA
I-	Quiescent Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	**-400**	-	**-**	µA
I+	Standby Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±10.8V, ±13.2V	-	-	**400**	µA
I-	Standby Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±10.8V, ±13.2V	**-400**	-	**-**	µA
I_{REF}	Supply Current Into V_{REF}	V_{REF} = 5.5V, V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	**-**	-	**35**	µA
DYNAMIC						
t_{ALH}	Transition Time	Figures 4, 5	-	0.5	**800**	ns
t_{AHL}	Transition Time	Figures 4, 5	-	0.5	**800**	ns
t_{BBM}	Break-Before-Make Delay	Figures 8, 9	**5**	50	**200**	ns
		Post radiation	**5**	-	**400**	ns
t_{ENABLE}	Enable Turn-On Time	Figures 6, 7	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns
$t_{DISABLE}$	Disable Turn-Off Time	Figures 6, 7	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

TABLE 2. TRUTH TABLE

A4	A3	A2	A1	A0	EN	“ON”-CHANNEL
X	X	X	X	X	1	None
0	0	0	0	0	0	1
0	0	0	0	1	0	2
0	0	0	1	0	0	3
0	0	0	1	1	0	4
0	0	1	0	0	0	5
0	0	1	0	1	0	6
0	0	1	1	0	0	7
0	0	1	1	1	0	8
0	1	0	0	0	0	9
0	1	0	0	1	0	10
0	1	0	1	0	0	11
0	1	0	1	1	0	12
0	1	1	0	0	0	13
0	1	1	0	1	0	14
0	1	1	1	0	0	15
0	1	1	1	1	0	16
1	0	0	0	0	0	17
1	0	0	0	1	0	18
1	0	0	1	0	0	19
1	0	0	1	1	0	20
1	0	1	0	0	0	21
1	0	1	0	1	0	22
1	0	1	1	0	0	23
1	0	1	1	1	0	24
1	1	0	0	0	0	25
1	1	0	0	1	0	26
1	1	0	1	0	0	27
1	1	0	1	1	0	28
1	1	1	0	0	0	29
1	1	1	0	1	0	30
1	1	1	1	0	0	31
1	1	1	1	1	0	32

Note: X = Don’t care, “1” = Logic High, “0” = Logic Low

Block Diagram

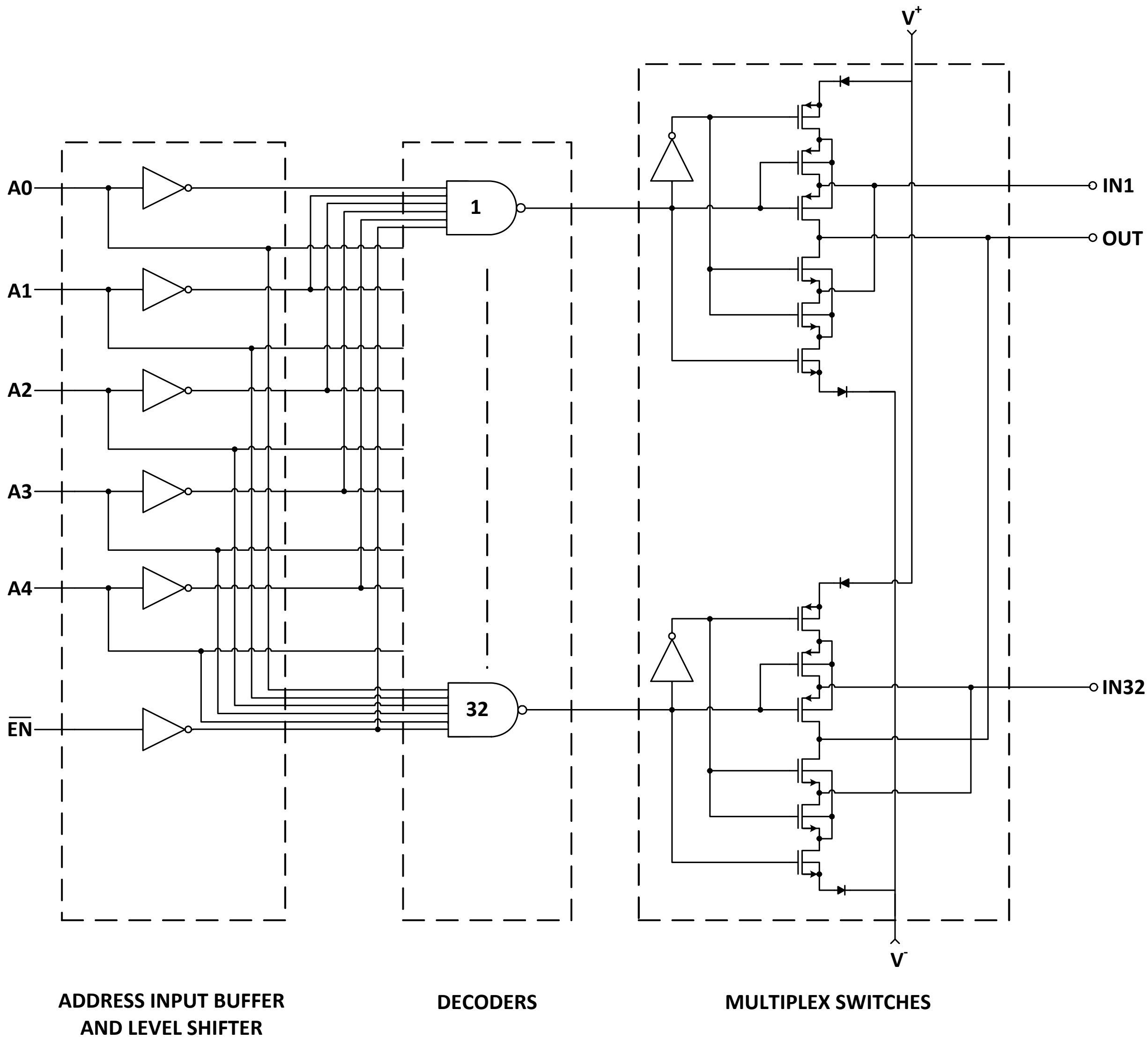


FIGURE 3. BLOCK DIAGRAM

Timing Diagrams

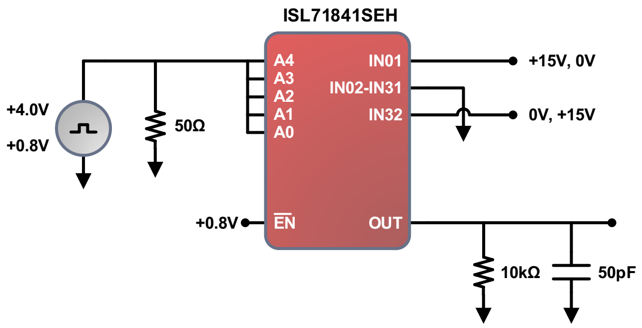


FIGURE 4. ADDRESS TIME TO OUTPUT TEST CIRCUIT

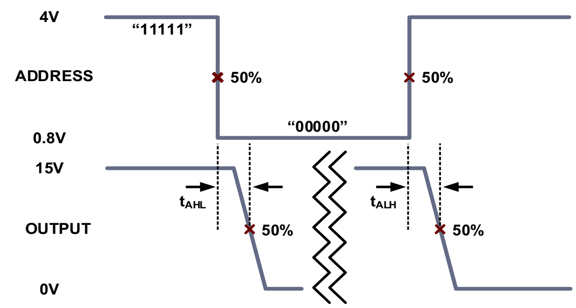


FIGURE 5. ADDRESS TIME TO OUTPUT DIAGRAM

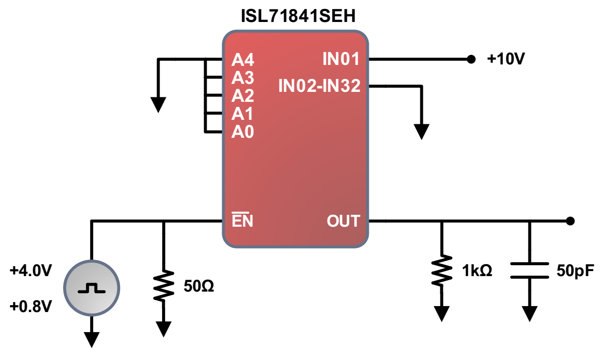


FIGURE 6. TIME TO ENABLE/DISABLE OUTPUT TEST CIRCUIT

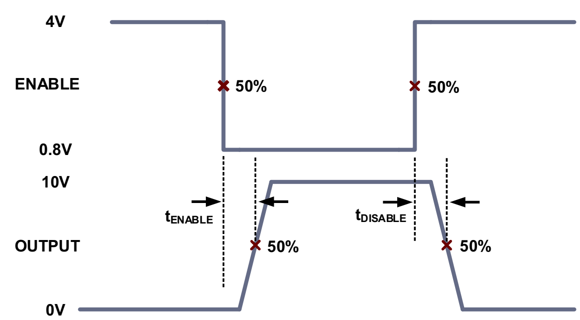


FIGURE 7. TIME TO ENABLE/DISABLE OUTPUT DIAGRAM

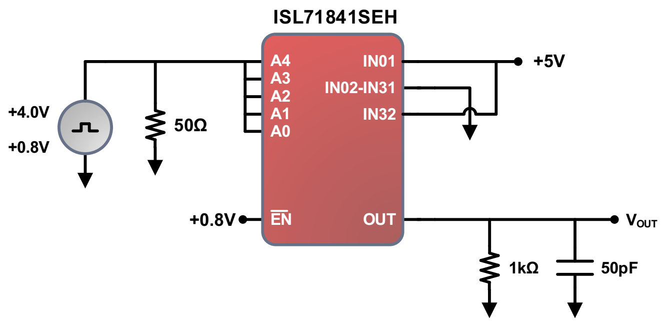


FIGURE 8. BREAK-BEFORE-MAKE TEST CIRCUIT

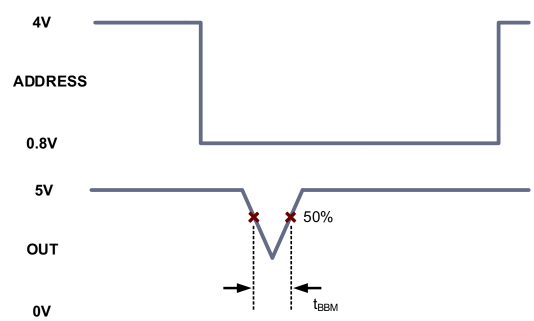


FIGURE 9. BREAK-BEFORE-MAKE DIAGRAM

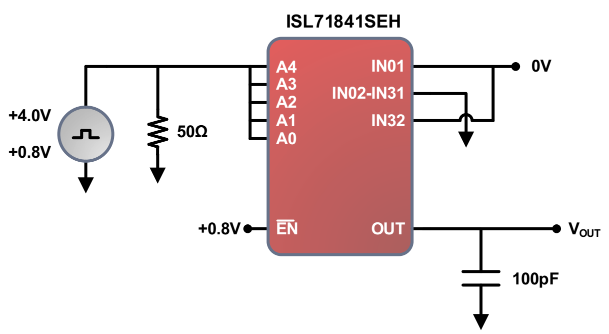


FIGURE 10. CHARGE INJECTION TEST CIRCUIT

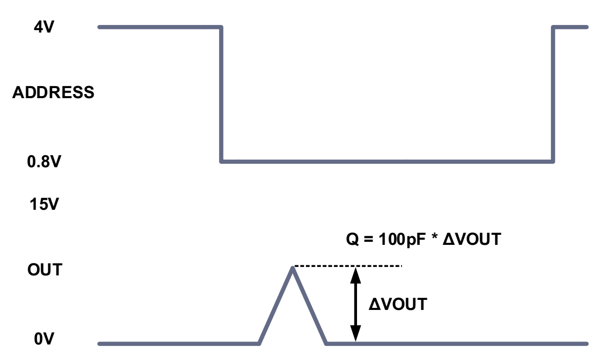


FIGURE 11. CHARGE INJECTION DIAGRAM

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified.

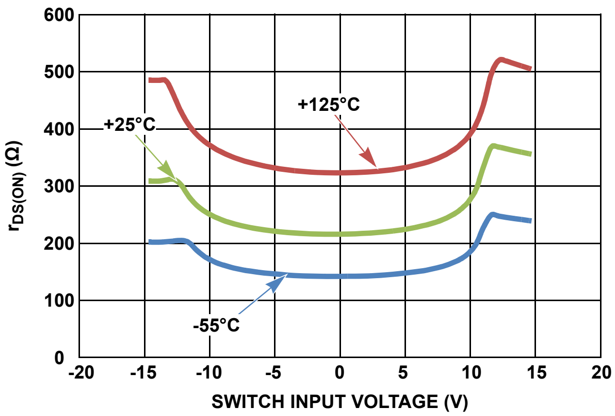


FIGURE 12. $r_{DS(ON)}$ vs VCM (V± = 14.5V)

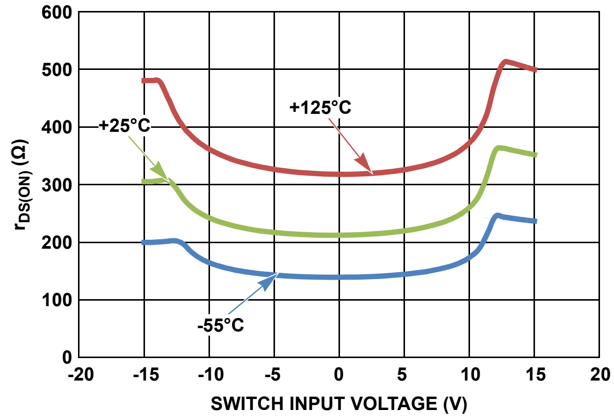


FIGURE 13. $r_{DS(ON)}$ vs VCM (V± = 15.0V)

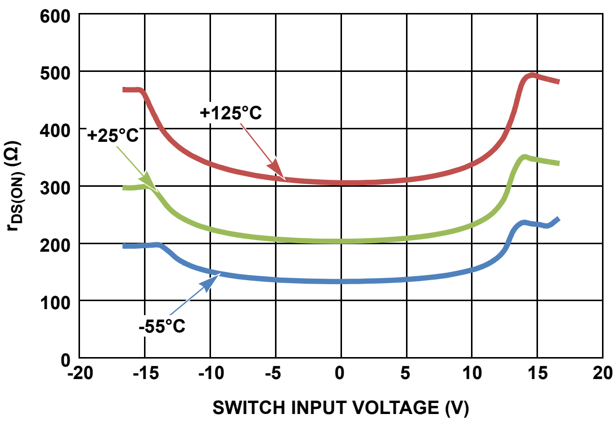


FIGURE 14. $r_{DS(ON)}$ vs VCM (V± = 16.5V)

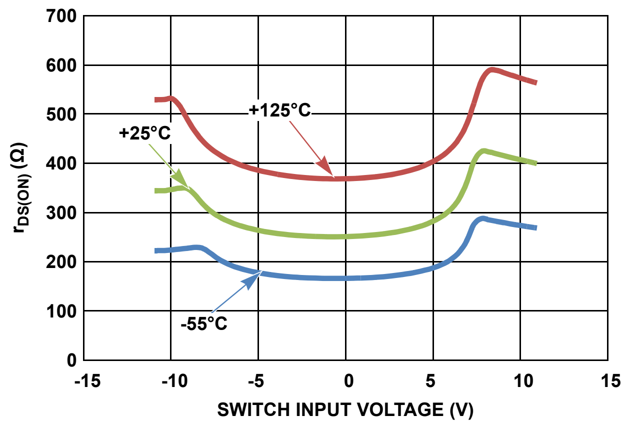


FIGURE 15. $r_{DS(ON)}$ vs VCM (V± = 10.8V)

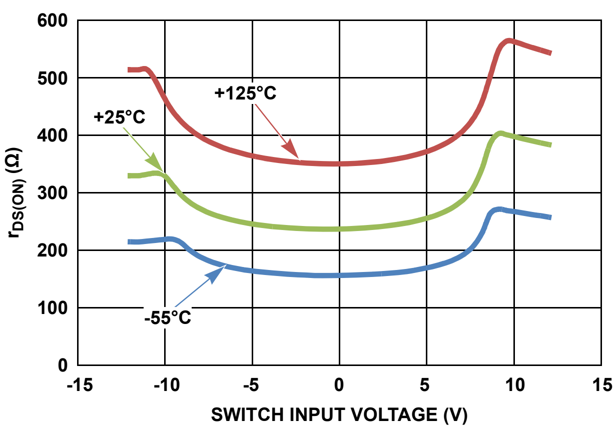


FIGURE 16. $r_{DS(ON)}$ vs VCM (V± = 12.0V)

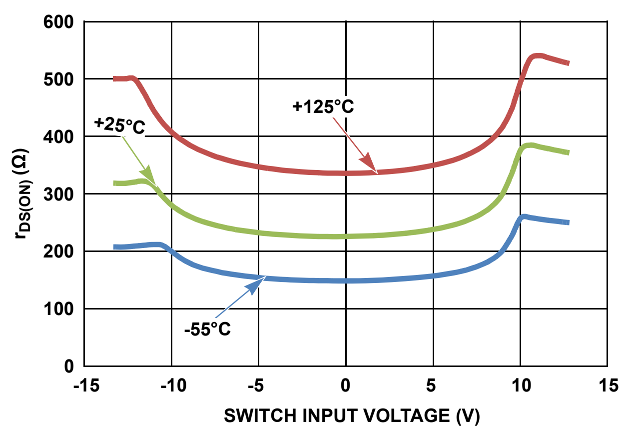


FIGURE 17. $r_{DS(ON)}$ vs VCM (V± = 13.2V)

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Continued)

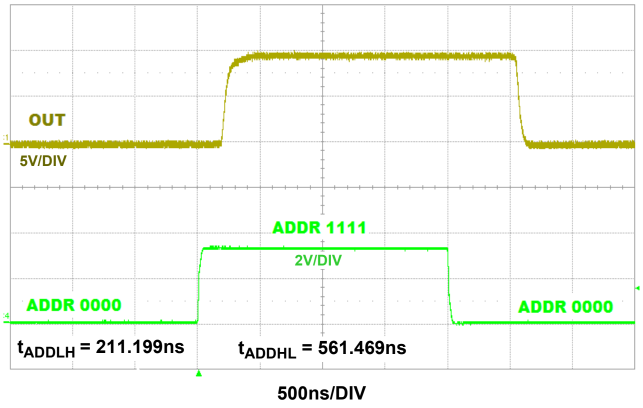


FIGURE 18. TYPICAL ADDRESS TO OUTPUT DELAY (V± = ±15V, +25°C)

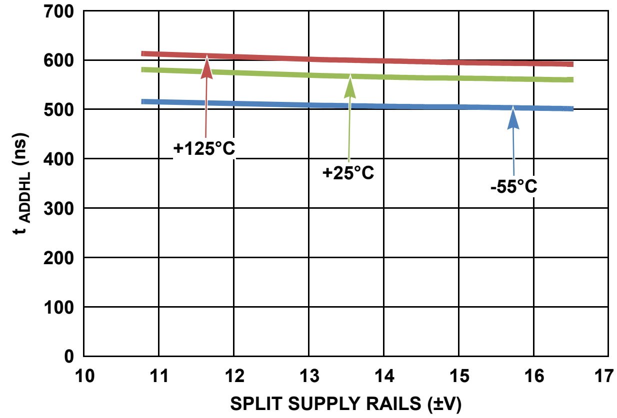


FIGURE 19. ADDRESS TO OUTPUT DELAY (HIGH TO LOW)

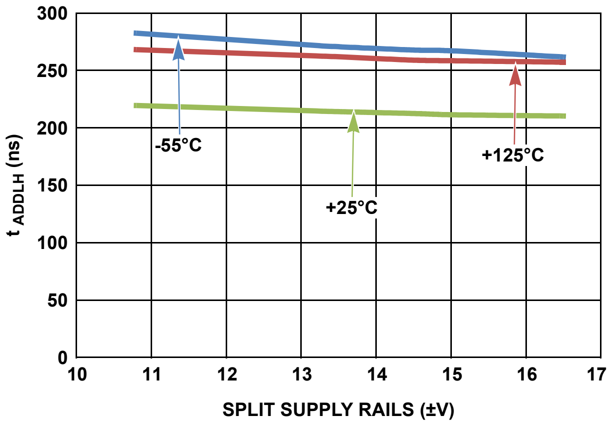


FIGURE 20. ADDRESS TO OUTPUT DELAY (LOW TO HIGH)

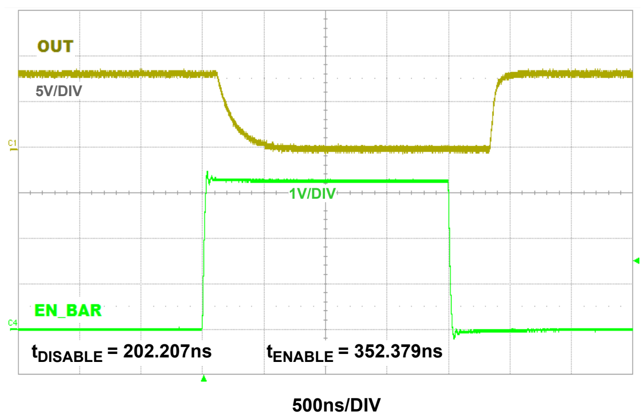


FIGURE 21. TYPICAL ENABLE TO OUTPUT DELAY (V± = ±15V, +25°C)

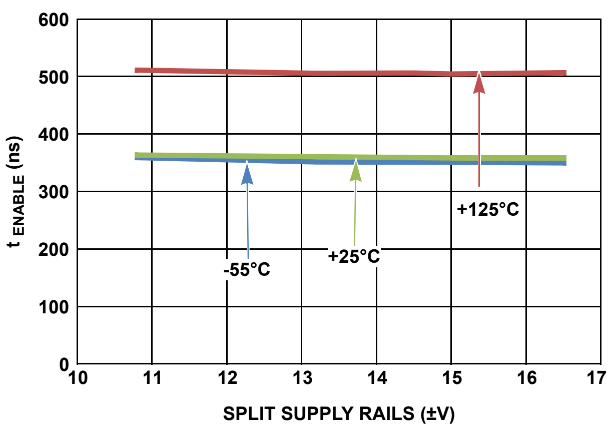


FIGURE 22. ENABLE TO OUTPUT DELAY (LOW TO HIGH)

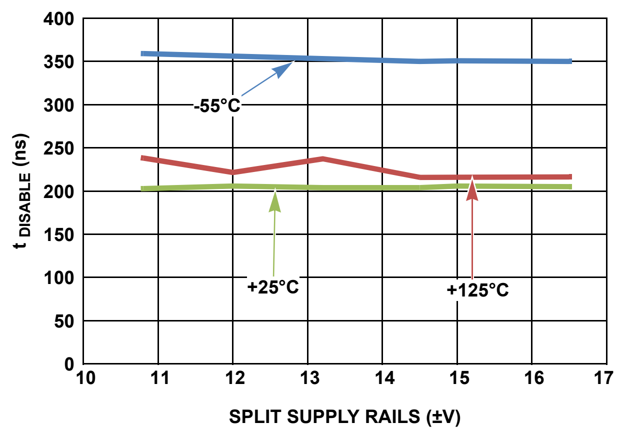


FIGURE 23. DISABLE TO OUTPUT DELAY (LOW TO HIGH)

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Continued)

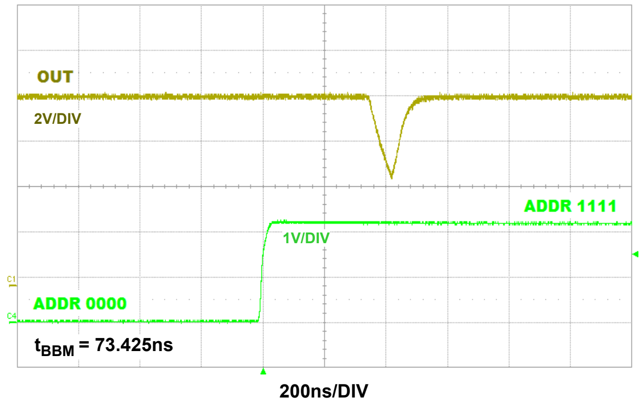


FIGURE 24. TYPICAL BREAK-BEFORE-MAKE DELAY (V± = 15V, +25°C)

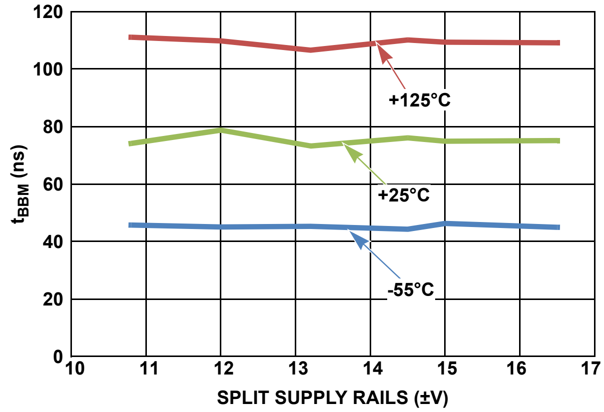


FIGURE 25. BREAK-BEFORE-MAKE DELAY

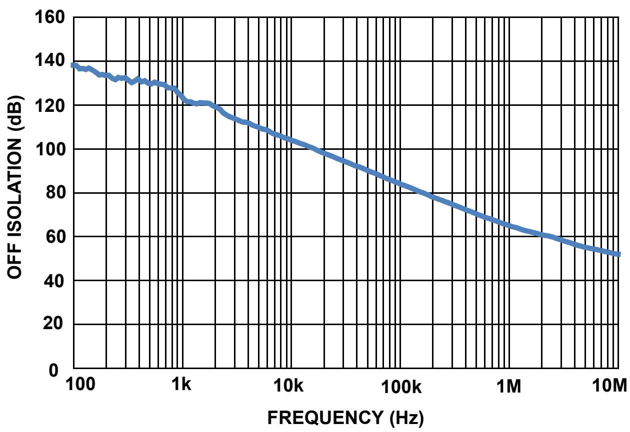


FIGURE 26. OFF ISOLATION (V± = ±15V, R_L = 1kΩ, +25°C)

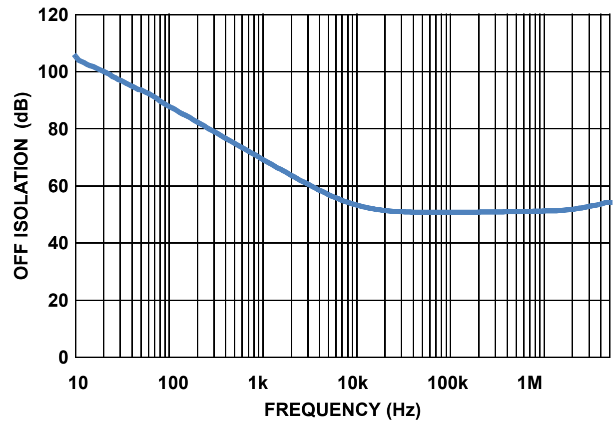


FIGURE 27. OFF ISOLATION (V± = ±15V, R_L = OPEN, +25°C)

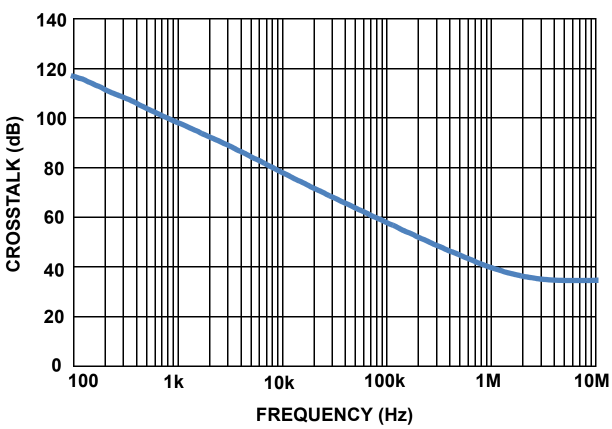


FIGURE 28. CROSSTALK (V± = ±15V, R_L = 1kΩ, +25°C)

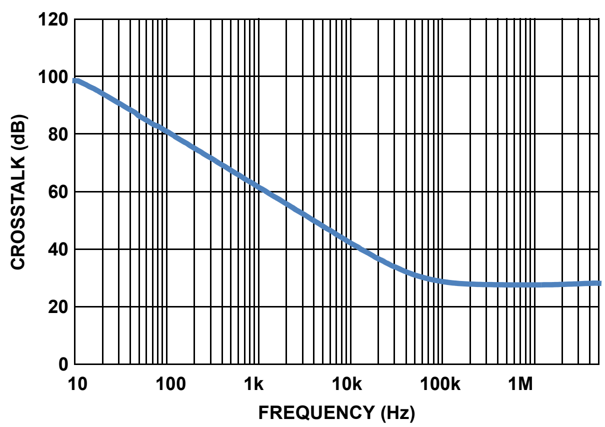


FIGURE 29. CROSSTALK (V± = ±15V, R_L = OPEN, +25°C)

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

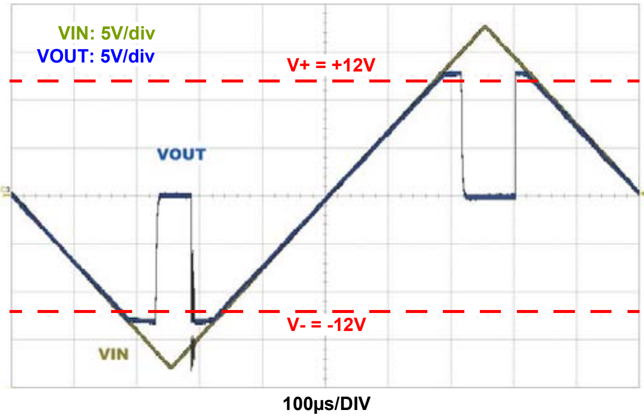


FIGURE 30. OVERVOLTAGE/UNDERVOLTAGE PROTECTION (+25°C)

Post High Dose Rate Radiation Characteristics (V_S = ±15V) Unless otherwise specified, V_S = ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

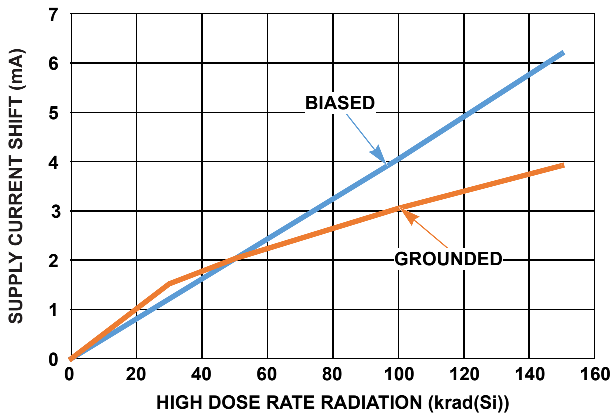


FIGURE 31. I_{CC} SUPPLY CURRENT SHIFT vs HDR RADIATION

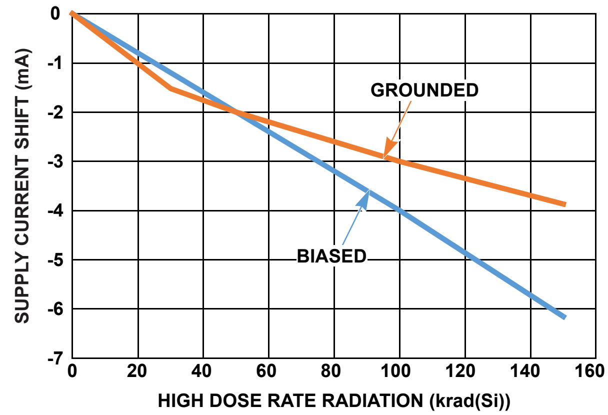


FIGURE 32. I_{EE} SUPPLY CURRENT SHIFT vs HDR RADIATION

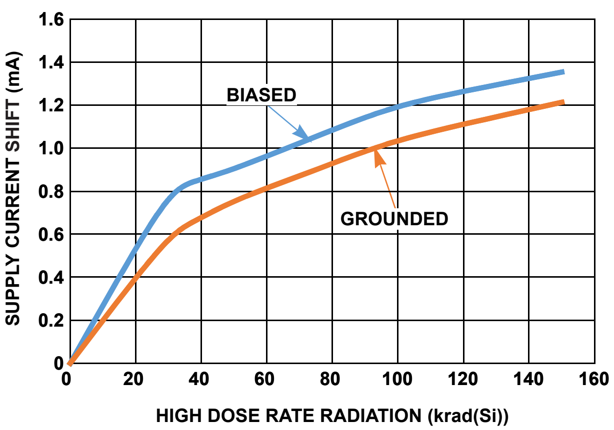


FIGURE 33. I_{REF} SUPPLY CURRENT SHIFT vs HDR RADIATION

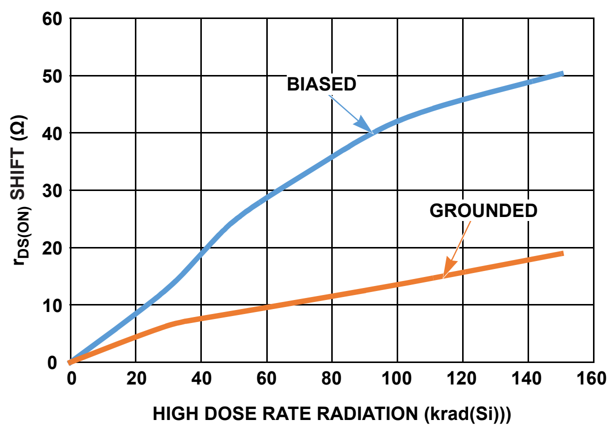


FIGURE 34. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs HDR RADIATION

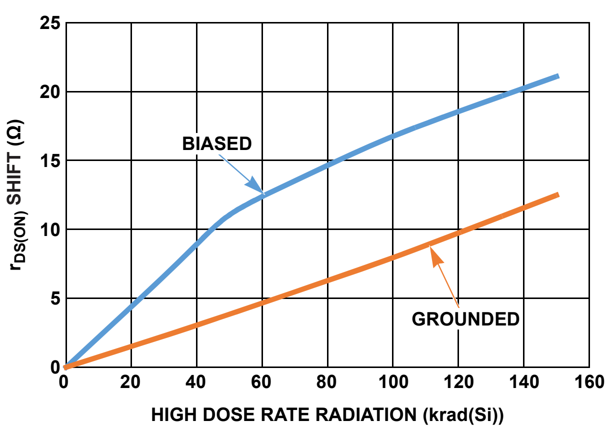


FIGURE 35. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs HDR RADIATION

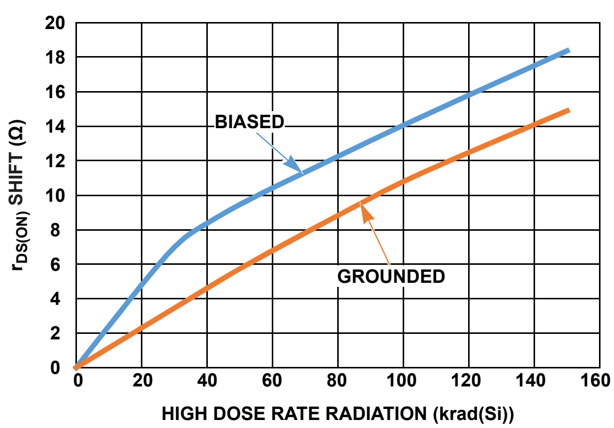


FIGURE 36. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs HDR RADIATION

Post High Dose Rate Radiation Characteristics (V_S = ±15V) Unless otherwise specified, V_S = ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. (Continued)

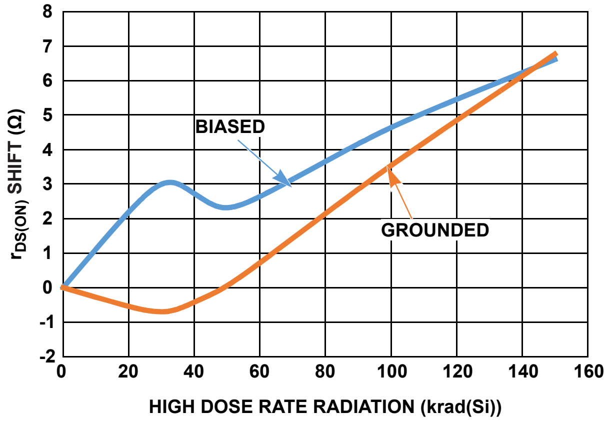


FIGURE 37. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs HDR RADIATION

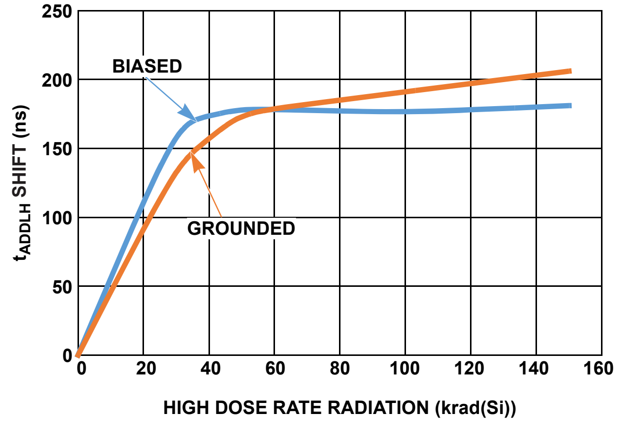


FIGURE 38. t_{ADD} SHIFT (LOW TO HIGH) vs HDR RADIATION

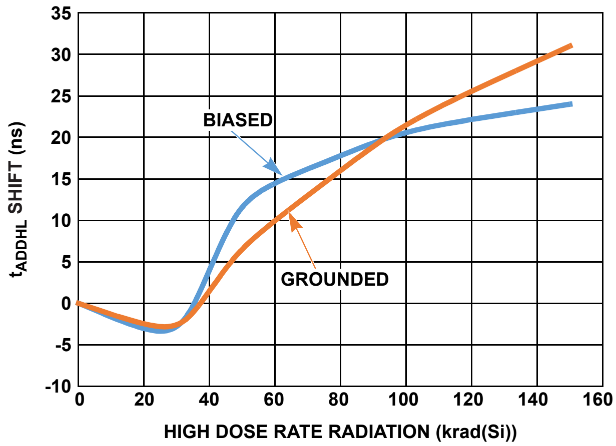


FIGURE 39. t_{ADD} SHIFT (HIGH TO LOW) vs HDR RADIATION

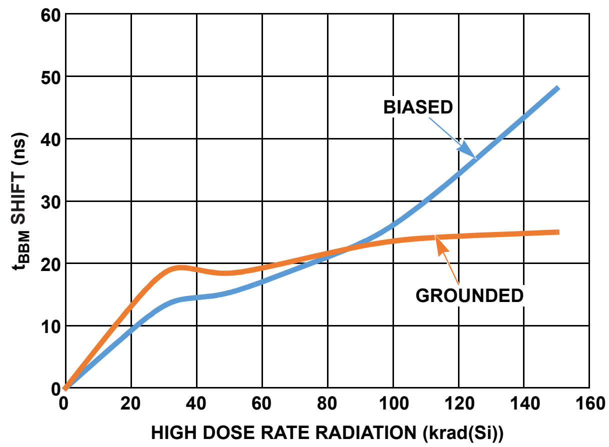


FIGURE 40. t_{BBM} SHIFT vs HDR RADIATION

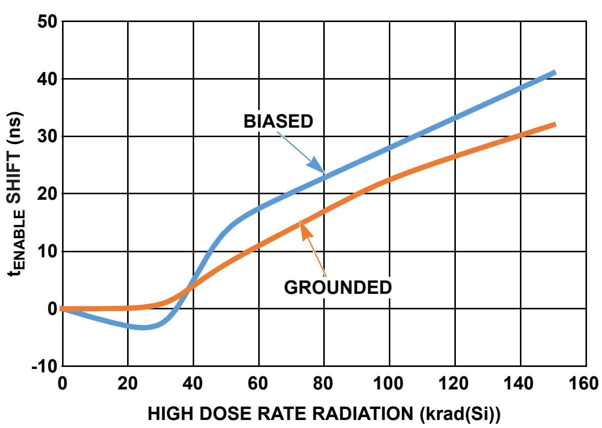


FIGURE 41. t_{ENABLE} SHIFT vs HDR RADIATION

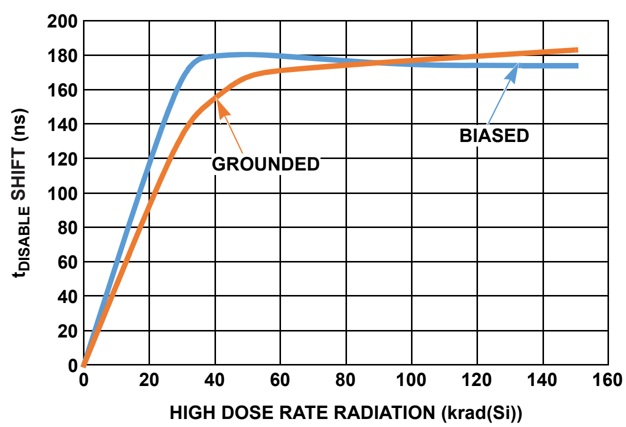


FIGURE 42. $t_{DISABLE}$ SHIFT vs HDR RADIATION

Post High Dose Rate Radiation Characteristics (V_S = ±12V) Unless otherwise specified, V_S = ± 12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

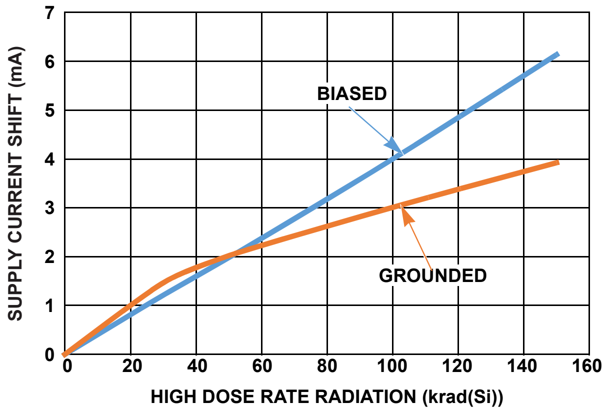


FIGURE 43. I_{CC} SUPPLY CURRENT SHIFT vs HDR RADIATION

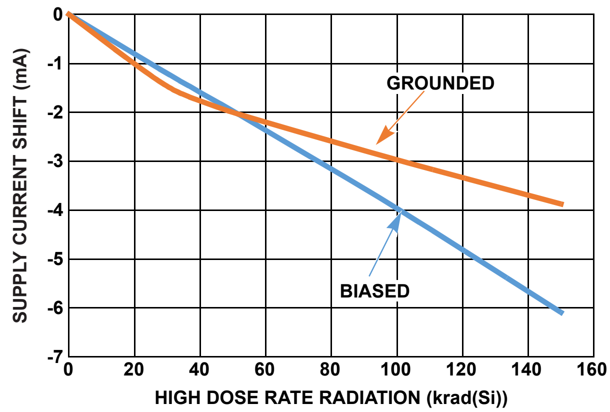


FIGURE 44. I_{EE} SUPPLY CURRENT SHIFT vs HDR RADIATION

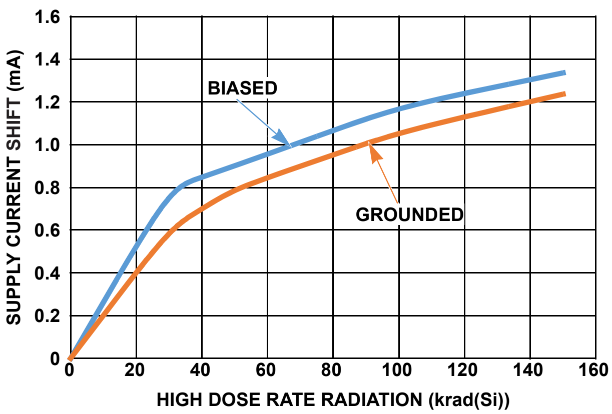


FIGURE 45. I_{REF} SUPPLY CURRENT SHIFT vs HDR RADIATION

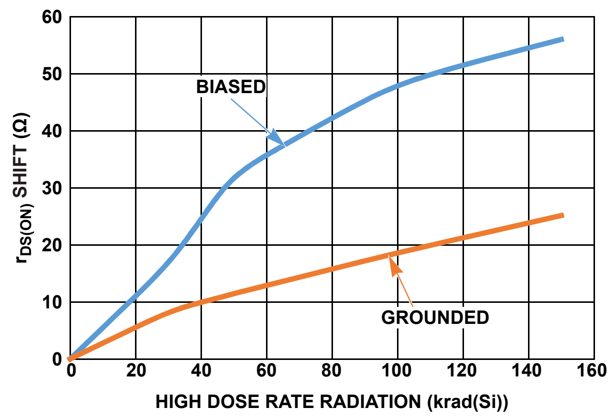


FIGURE 46. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs HDR RADIATION

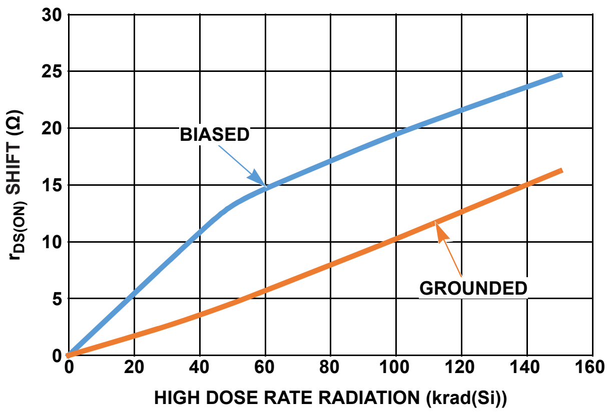


FIGURE 47. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs HDR RADIATION

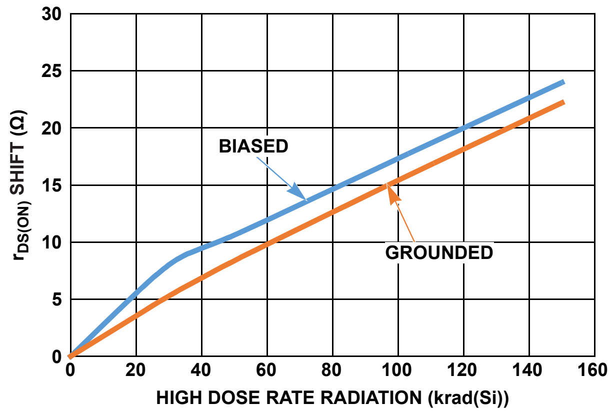


FIGURE 48. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs HDR RADIATION

Post High Dose Rate Radiation Characteristics (V_S = ±12V)

Unless otherwise specified, V_S = ± 12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

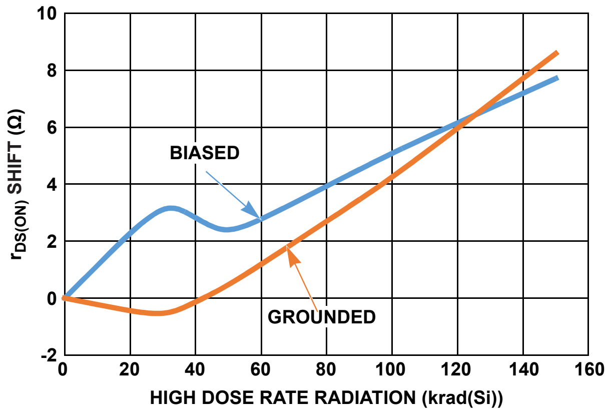


FIGURE 49. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs HDR RADIATION

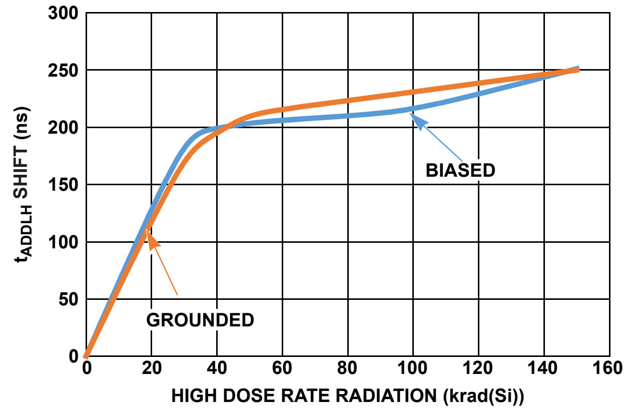


FIGURE 50. t_{ADD} SHIFT (LOW TO HIGH) vs HDR RADIATION

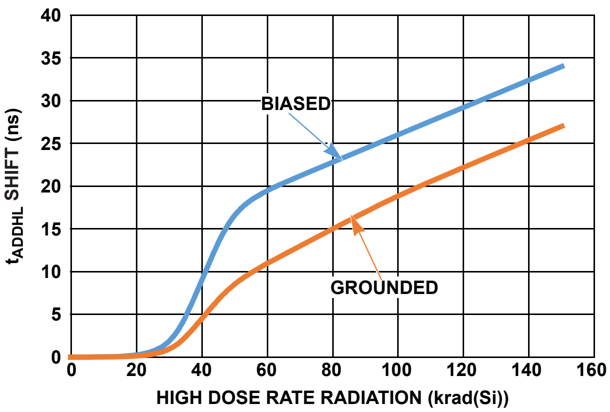


FIGURE 51. t_{ADD} SHIFT (HIGH TO LOW) vs HDR RADIATION

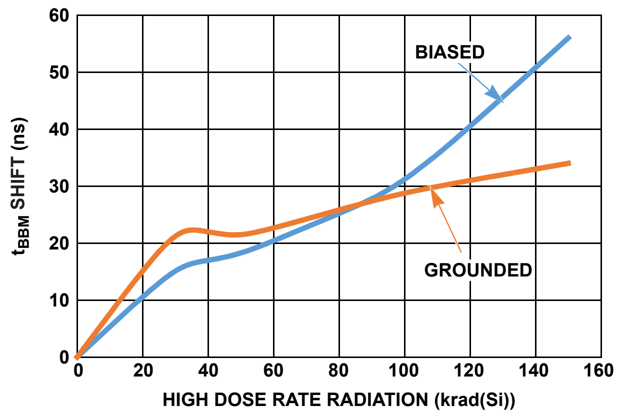


FIGURE 52. t_{BBM} SHIFT vs HDR RADIATION

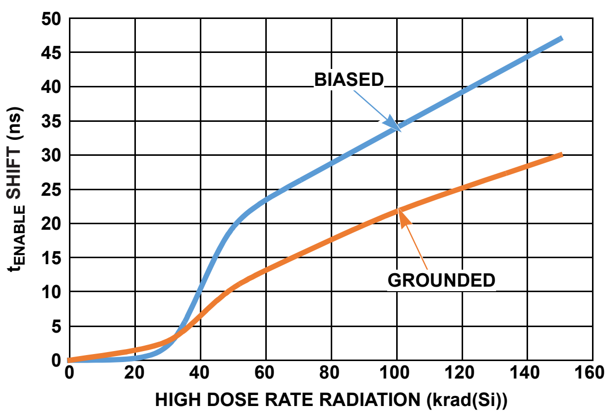


FIGURE 53. t_{ENABLE} SHIFT vs HDR RADIATION

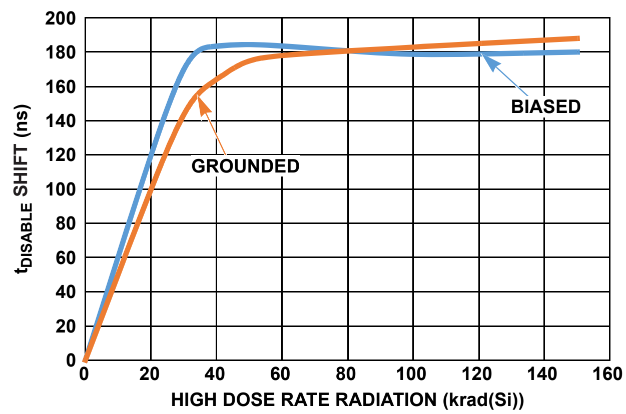


FIGURE 54. $t_{DISABLE}$ SHIFT vs HDR RADIATION

Post Low Dose Rate Radiation Characteristics (V_S = ±15V)

Unless otherwise specified, V_S = ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

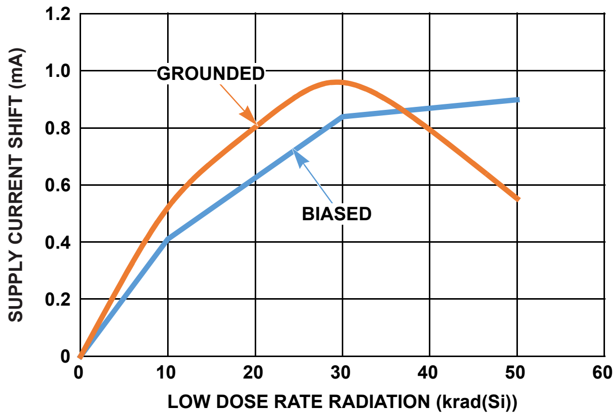


FIGURE 55. I_{CC} SUPPLY CURRENT SHIFT vs LDR RADIATION

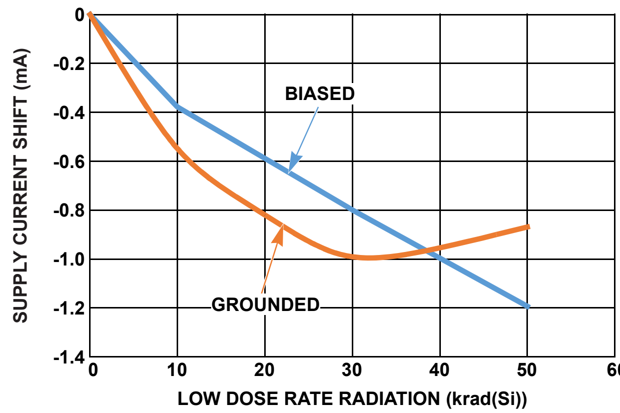


FIGURE 56. I_{EE} SUPPLY CURRENT SHIFT vs LDR RADIATION

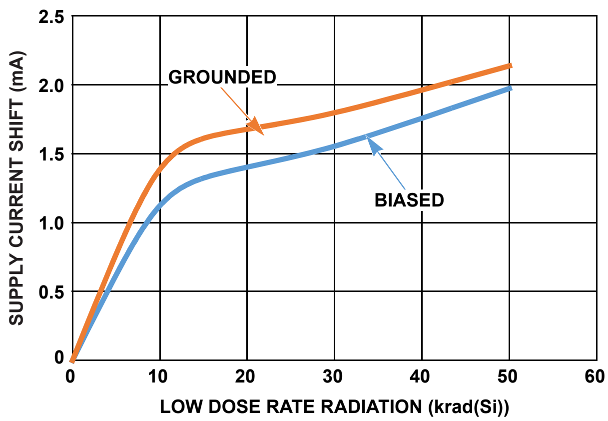


FIGURE 57. I_{REF} SUPPLY CURRENT SHIFT vs LDR RADIATION

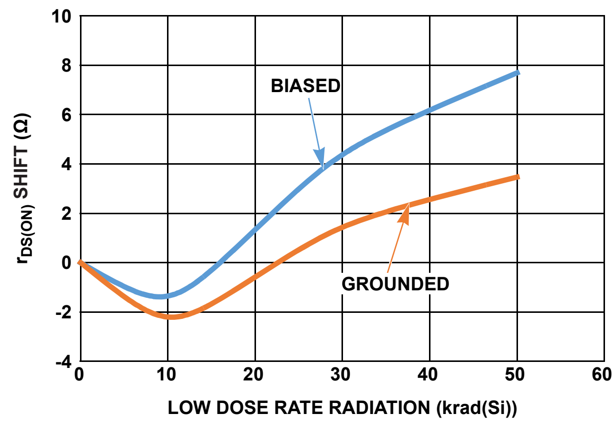


FIGURE 58. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs LDR RADIATION

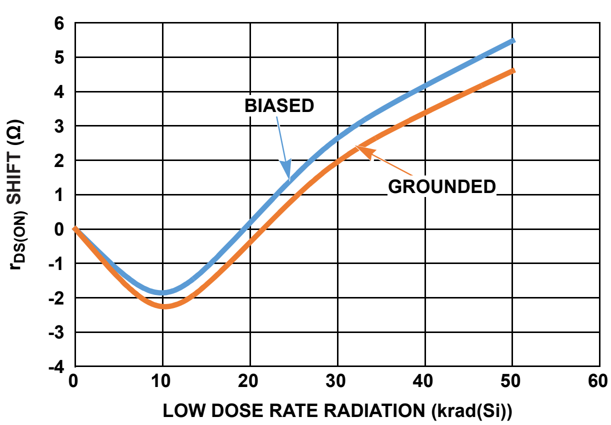


FIGURE 59. $r_{DS(ON)}$ Shift (V_{IN} = -5V) vs LDR RADIATION

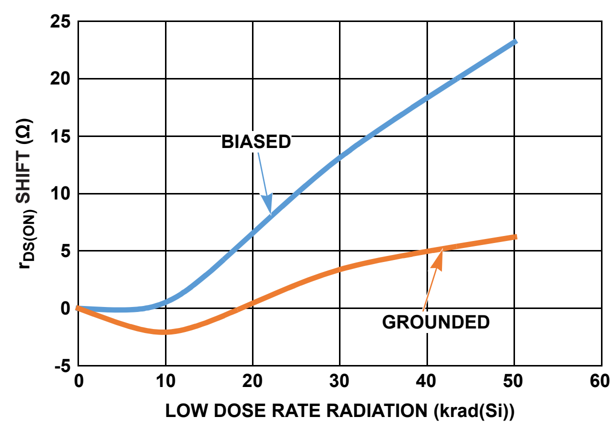


FIGURE 60. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V_S = ±15V)

Unless otherwise specified, V_S = ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

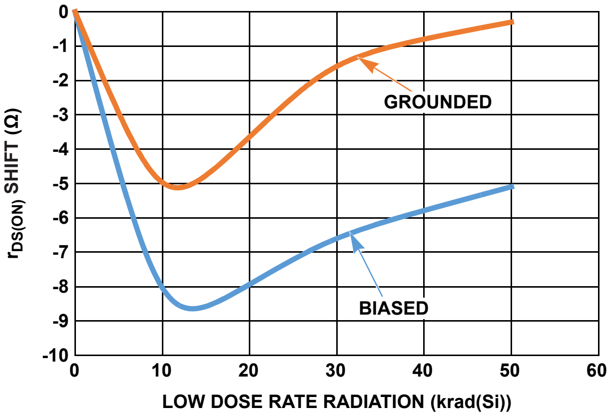


FIGURE 61. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs LDR RADIATION

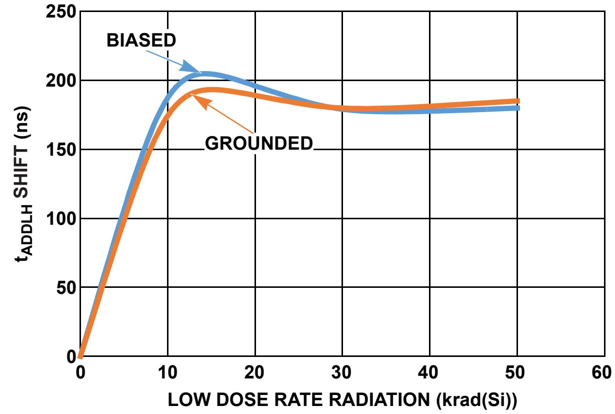


FIGURE 62. t_{ADD} SHIFT (LOW TO HIGH) vs LDR RADIATION

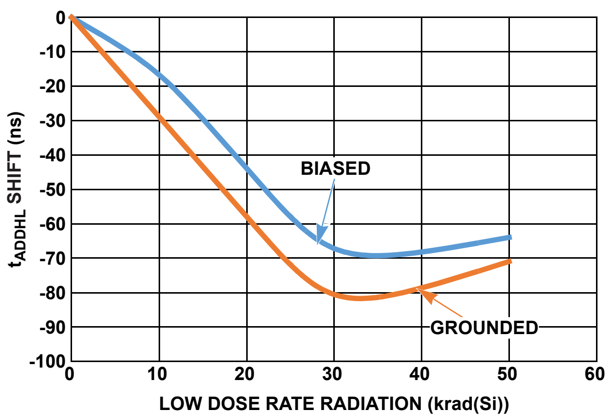


FIGURE 63. t_{ADD} SHIFT (HIGH TO LOW) vs LDR RADIATION

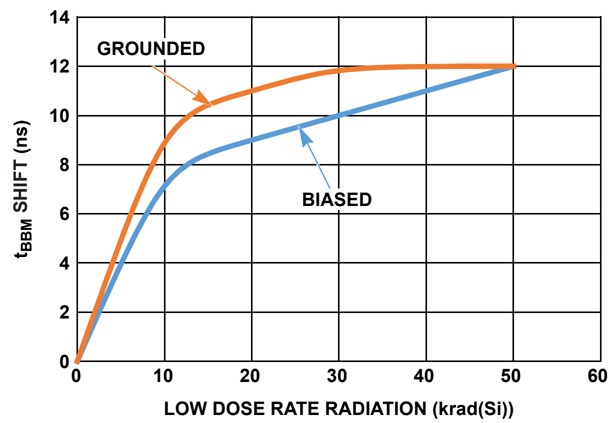


FIGURE 64. t_{BBM} SHIFT vs LDR RADIATION

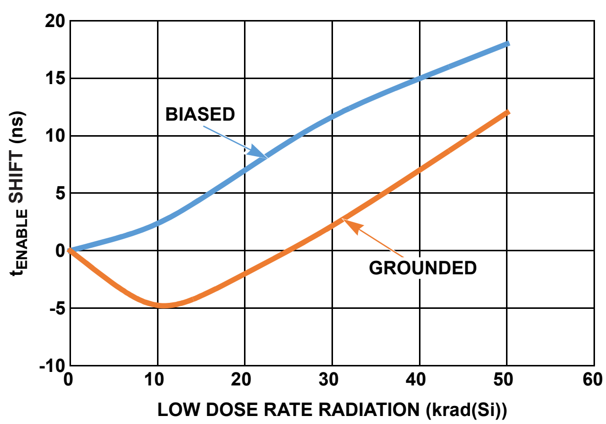


FIGURE 65. t_{ENABLE} SHIFT vs LDR RADIATION

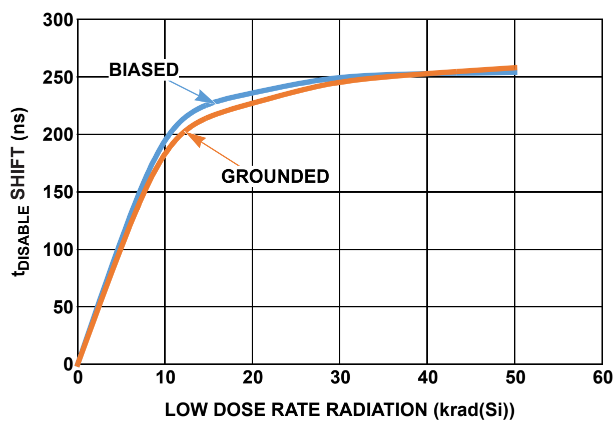


FIGURE 66. $t_{DISABLE}$ SHIFT vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V_S = ±12V)

Unless otherwise specified, V_S = ± 12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

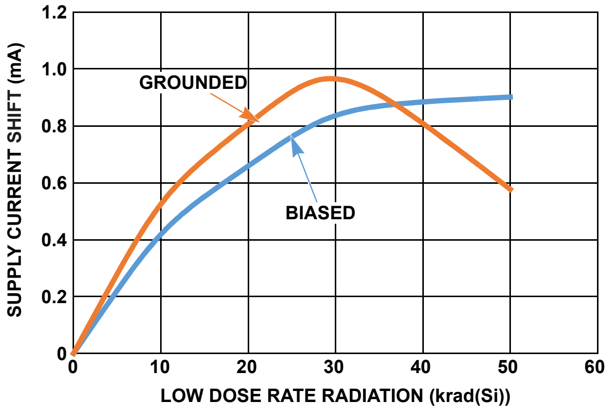


FIGURE 67. I_{CC} SUPPLY CURRENT SHIFT vs LDR RADIATION

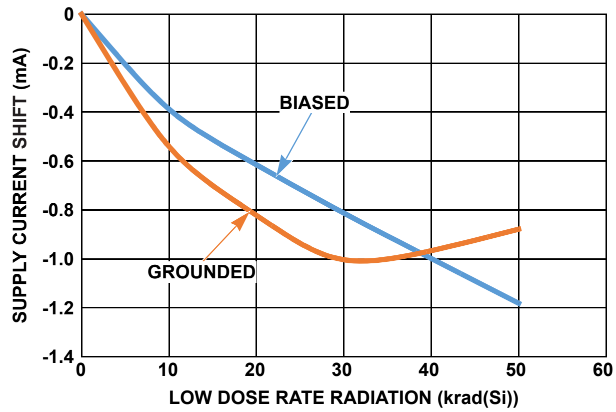


FIGURE 68. I_{EE} SUPPLY CURRENT SHIFT vs LDR RADIATION

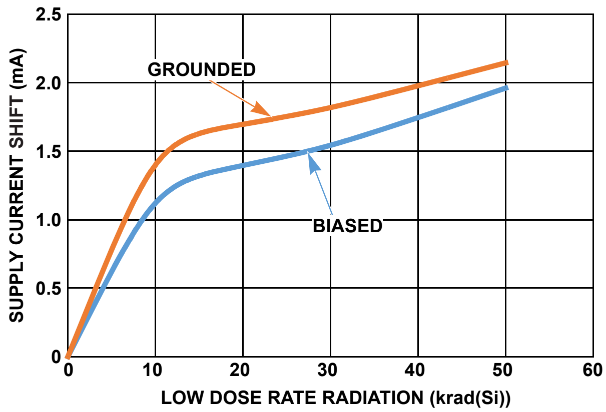


FIGURE 69. I_{REF} SUPPLY CURRENT SHIFT vs LDR RADIATION

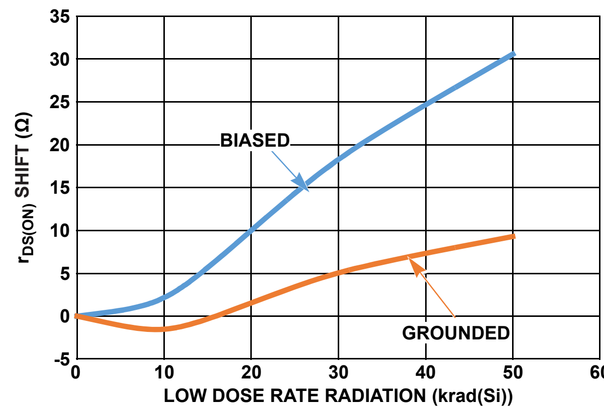


FIGURE 70. $r_{DS(ON)}$ SHIFT ($V_{IN} = V^+$) vs LDR RADIATION

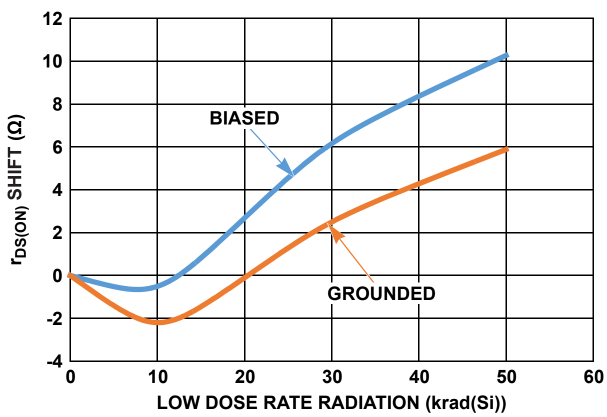


FIGURE 71. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs LDR RADIATION

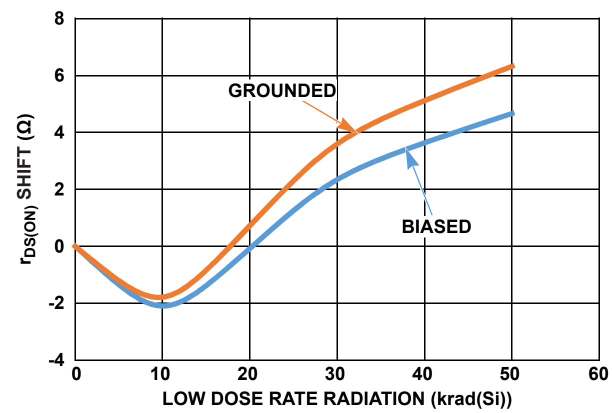


FIGURE 72. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V_S = ±12V)

Unless otherwise specified, V_S = ± 12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

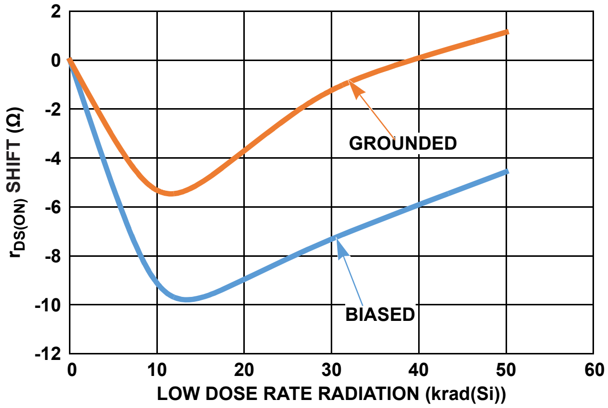


FIGURE 73. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs LDR RADIATION

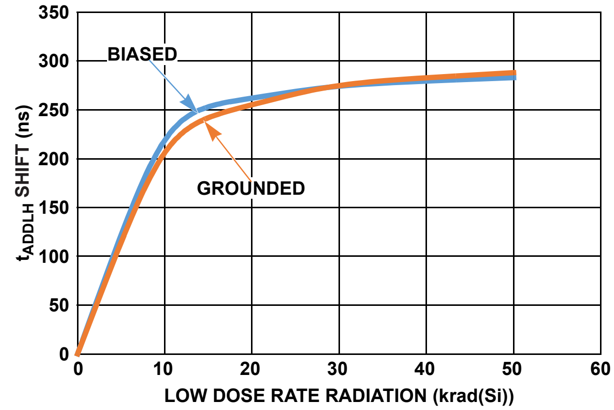


FIGURE 74. t_{ADD} SHIFT (LOW TO HIGH) vs LDR RADIATION

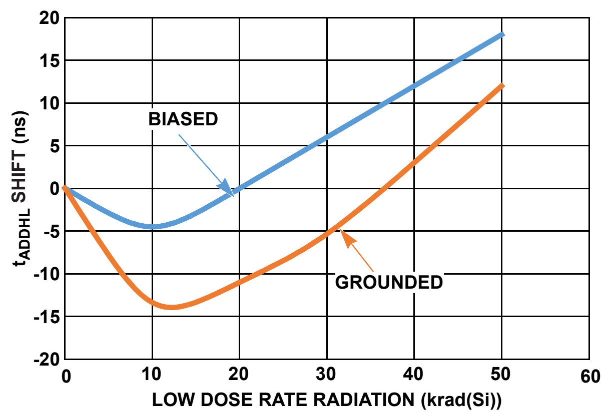


FIGURE 75. t_{ADD} SHIFT (HIGH TO LOW) vs LDR RADIATION

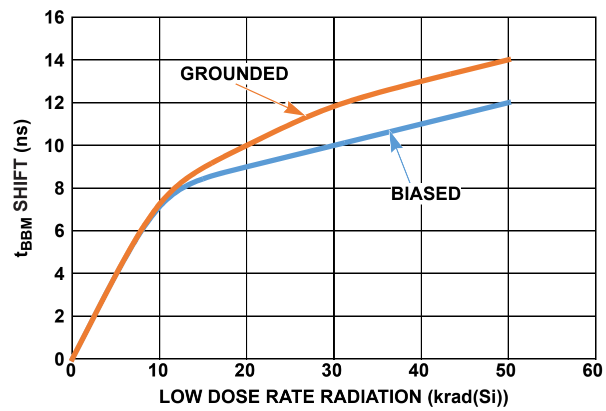


FIGURE 76. t_{BBM} SHIFT vs LDR RADIATION

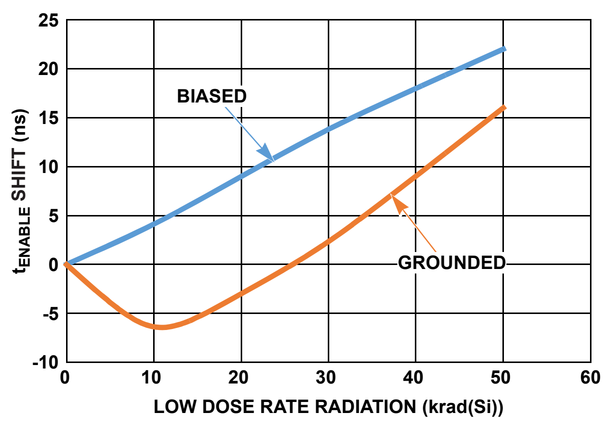


FIGURE 77. t_{ENABLE} SHIFT vs LDR RADIATION

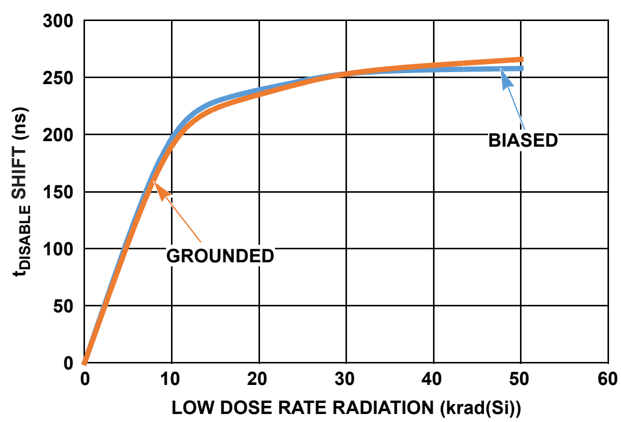


FIGURE 78. $t_{DISABLE}$ SHIFT vs LDR RADIATION

Applications Information

Power-Up Considerations

The circuit is designed to be insensitive to any given power-up sequence between V^+, V^- and VREF, however, it is recommended that all supplies power-up relatively close to each other.

Overvoltage Protection

The ISL71841SEH has overvoltage protection on both the input as well as the output. On the output, the voltage is limited to a diode past the rails. Each of the inputs has independent overvoltage protection that works regardless of the switch being selected. If a switch experiences an overvoltage condition (3-4V) past the rail), the switch is turned off. As soon as the voltage returns within the rails, the switch returns to normal operation.

VREF and Logic Functionality

The VREF pin sets the logic threshold for the ISL71841SEH. The range for VREF is between 4.5V and 5.5V with a nominal voltage of 5V. The address pins and enable are compared against roughly 30% of V_{REF} voltage (refer to Figure 79). With 5.0V on V_{REF}, the switching point is set to around 1.4V. This switching point allows for both 5V and 3.3V logic control.

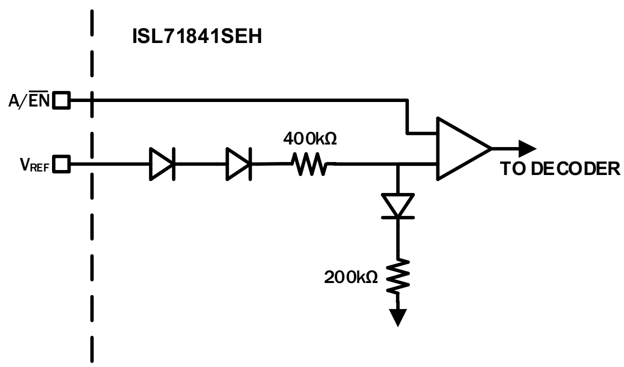


FIGURE 79. SIMPLIFIED V_{REF} CIRCUITRY

ISL71841SEH vs ISL71840SEH

There is a 16-channel version of the ISL71841SEH available in a 28 Ld CDFP. In terms of performance specs, the parts are very similar in behavior. Apart from the apparent increase in channel density, the ISL71841SEH does have slightly higher output leakage compared to the ISL71840SEH due to having more channels connected to the output. The supply current for the ISL71841SEH is also a bit higher compared to the ISL71840SEH. (See Table 1 on page 3.)

Die Characteristics

Die Dimensions

5000µm x 4080µm (197mils x 161mils)
Thickness: 483µm ± 25µm (19mils ± 1mil)

Interface Materials

GLASSIVATION

Type: 12kÅ Silicon Nitride on 3kÅ Oxide

TOP METALLIZATION

Type: 300Å TiN on 2.8µm AlCu
In Bondpads, TiN has been removed.

BACKSIDE FINISH

Silicon

PROCESS

P6SOI

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

1.6×10^5 A/cm^2

TRANSISTOR COUNT

10752

Weight of Packaged Device

1.54 grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Grounded, tied to package pin 29

Metalization Mask Layout

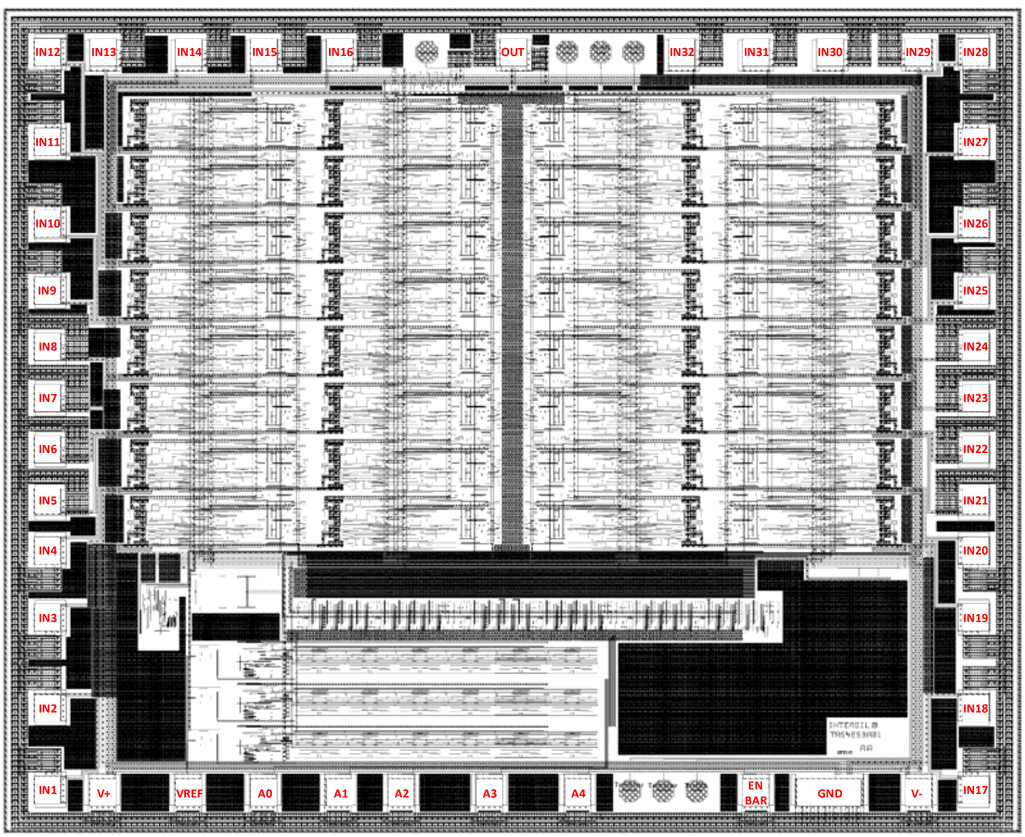


TABLE 3. ISL71840SEH DIE LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	PACKAGING PIN	ΔX (µm)	ΔY (µm)	X (µm)	Y (µm)
1	IN28	P42	122	122	2232.2	1776.05
2	IN29	P43	122	122	1956.5	1772.2
3	IN30	P44	122	122	1529.15	1772.2
4	IN31	P45	122	122	1171.85	1772.2
5	IN32	P46	122	122	816.35	1772.2
9	OUT	P1	122	122	7.2	1773.25
11	IN16	P3	122	122.05	-829.525	1772.2
12	IN15	P4	122	122	-1192.2	1772.2
13	IN14	P5	122	122	-1553.65	1772.2
14	IN13	P6	122	122	-1965.35	1772.2
15	IN12	P7	122	122	-2232.2	1775.55
16	IN11	P8	122	122	-2232.2	1343.55
17	IN10	P9	122	122	-2232.2	944.5
18	IN9	P10	122	122	-2232.2	626.15
19	IN8	P11	122	122	-2232.2	354.4
20	IN7	P12	122	122.05	-2232.2	108.275
21	IN6	P13	122	122	-2232.2	-138.75
22	IN5	P14	122	122	-2232.2	-391.8
23	IN4	P15	122	122	-2232.2	-622.95
24	IN3	P16	122	122	-2232.2	-948.55
25	IN2	P17	122	122	-2232.2	-1379.95
26	IN1	P18	122	122	-2232.2	-1775.95
27	V^+	P19	122	122	-1970.75	-1789.2
28	VREF	P20	122	122	-1558.65	-1789.2
29	A0	P21	122	122	-1196.8	-1789.2
30	A1	P22	122	122	-835.6	-1789.2
31	A2	P23	122	122	-533	-1789.2
32	A3	P24	122	122	-109.45	-1789.2
33	A4	P25	122	122	313.95	-1789.2
37	EN_B	P28	122	122	1171.9	-1789.2
38	GND	P29,P29	320	122	1525.85	-1789.1
39	V^-	P30	122	122	1955.7	-1789.2
40	IN17	P31	122	122	2232.2	-1774.95
41	IN18	P32	122	122	2232.2	-1380.25
42	IN19	P33	122	122	2232.2	-947.45
43	IN20	P34	122	122	2232.2	-624.75
44	IN21	P35	122	122	2232.2	-391.95
45	IN22	P36	122	122	2232.2	-139.05
46	IN23	P37	122	122.05	2232.2	107.525

TABLE 3. ISL71840SEH DIE LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	PACKAGING PIN	ΔX (µm)	ΔY (µm)	X (µm)	Y (µm)
47	IN24	P38	122	122	2232.2	353.6
48	IN25	P39	122	122	2232.2	626.9
49	IN26	P40	122	122	2232.2	943.9
50	IN27	P41	122	122	2232.2	1342.7

NOTE: Origin of coordinates is the center of the die.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 11, 2015	FN8735.2	Updated Y-axis labels on Figures 31 through 78. Updated crosstalk and off Isolation MIN in Electrical Spec table on page 7 from -75 to 75 (off isolation) and -47 to 47 (crosstalk). Changed all instances of V_{DD} to V^+ and V_{SS} to V^-.
September 29, 2015	FN8735.1	Updated Related Literature on page 1. Updated testing information for ESD tolerances, HBM, CDM and MM in "Absolute Maximum Ratings" on page 5 From: Human Body Model (Tested per MIL-PRF-883 3015.7) Charged Device Model (Tested per MIL-PRF-883 3015.7) Machine Model (Tested per MIL-PRF-883 3015.7) To: Human Body Model (Tested per MIL-STD-883 TM 3015) Charged Device Model (Tested per JESD22-C101D) Machine Model (Tested per JESD22-A115-A) Updated crosstalk and off Isolation MIN in Electrical Spec table on page 7 from -90 to -75 (off isolation) and -47 (crosstalk) Added Figures 26, 28 and 30 and updated figure titles for Figures 27 and 29 on page 14. Updated top metalization thickness and composition in "Die Characteristics" on page 25. Added Table 3 on page 26.
June 11, 2015	FN8735.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

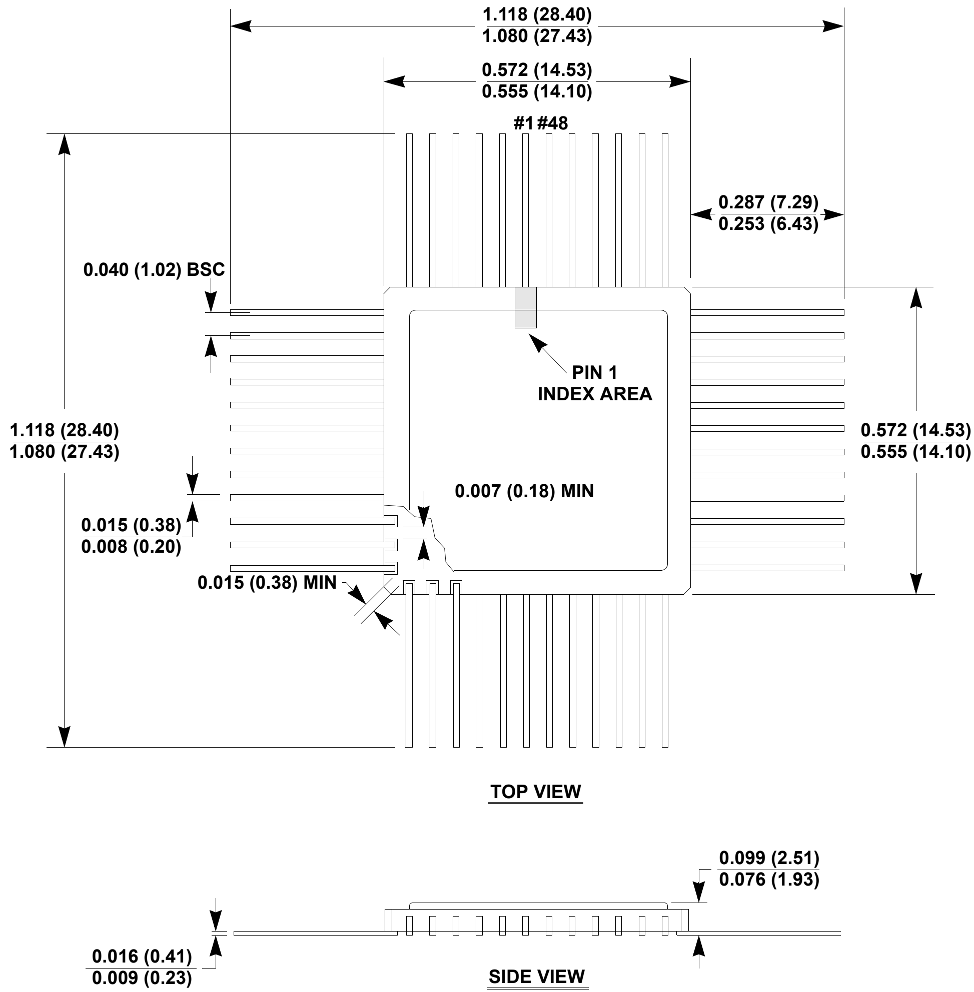
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

R48.A

48 CERAMIC QUAD FLATPACK PACKAGE (CQFP)

Rev 3, 10/12



NOTE:

1. All dimensions are in inches (millimeters).